REMARKS

The Title is herein amended, the Specification is herein amended, Claims 1, 3, 7, 12, 13, and 15 are herein amended, and Claim 20 is herein canceled, without prejudice, and the Abstract is herein amended to better encompass the full scope and breadth of the present invention, notwithstanding the Applicant's belief that the claims would have been allowable as originally filed. A marked-up version of the Specification, a marked-up version of the Claims, and a marked-up version of the Abstract are herewith submitted.

Specifically, independent Claims 1 and 12 are herein both amended by inserting wherein the first ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique, and wherein the second ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique. Dependent Claims 3 and 13 are herein both amended by deleting [wherein the first ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique,]. Dependent Claims 7 and 15 are herein both amended by deleting [wherein the second ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique,]. Claims 2, 4-6, 8-11, and 4-19 now subsume the limitations of the herein amended claims from which they depend. Therefore, reconsideration of the present application in light of the foregoing amendment and these remarks is respectfully requested.

I. Rejection of Claims 1, 2, 4-6, 8, 9, 11, 12, and 14 under 35 U.S.C. §102(b).

The Examiner has rejected Claims 1, 2, 4-6, 8, 9, 11, 12, and 14, under 35 U.S.C. §102(b), as being anticipated by Gardner et al. (US 5,963,810), stating:

> Gardner discloses the limitations of:
> ...
> depositing a first nitride film(303, fig. 3A) on a semiconductor substrate,
> depositing a high-k material (305, fig. 3B) on the first nitride (col. 5, lns. 30-64 and col. 3, lns. 25-32),
> depositing a second nitride film on the high-k material (col. 6, lns. 13-20); and
> completing fabrication of the device (col. 6, lns. 1-12).

Notwithstanding Claims 1, 3, 7, 12, 13, and 15 being herein amended to better encompass the present invention, the Applicant respectfully traverses the Examiner's grounds for rejection on this basis. Gardner merely teaches depositing a silicon nitride (Si_3N_4) layer 303 and an optional silicon nitride capping layer by **sputtering** (col. 5, ll. 30-45; col. 6, ll. 40-42). In

contrast, the Applicant teaches depositing silicon nitride layers 21 and 22 by an **atomic layer deposition (ALD)** technique (Spec., p. 3, l. 13, 20-21; herein amended Claims 1 and 12). As such, Gardner does not teach the presently claimed combination of method steps.

In addition, Gardner merely teaches a high dielectric constant material layer or high permittivity layer 305, comprising **barium strontium titanate ($Ba_{1-x}Sr_xO3$), tantalum oxide (Ta_xO_y), lead zinc niobate ($PbZn_xNb_{1-x}O_3$), and lead scandium tantalum oxide ($PbSc_xTa_{1-x}O_3$)**. In contrast, Claims 5, 6, and 14 collectively have the following limitation for forming the high dielectric constant material layer or thin metal film 30 which contains species not taught by Gardner: wherein the **thin metal film** comprises at least one metal selected from a group consisting essentially of **zirconium (Zr), hafnium (Hf), titanium (Ti), and tantalum (Ta)**, and wherein the **thin metal film** comprises **a metal oxide**. As such, the presently claimed thin metal film 30 **contains a distinct** group of species *in combination with* **depositing silicon nitride layers** 21 and 22 by an **atomic layer deposition (ALD)** technique.

Thus, Gardner does not teach the present combination of method steps respectively recited in Claims 1 and 12:

> 1. **(Amended)** A method of fabricating a semiconductor device, having a nitride/high-k material/nitride gate dielectric stack, comprising:
> initiating formation of the nitride/high-k material/nitride gate dielectric stack by:
> depositing **a first ultra-thin nitride film** on a semiconductor substrate, wherein the first ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique;
> depositing **a high-k material** on the first ultra-thin nitride film; and
> depositing **a second ultra-thin nitride film** on the high-k material, thereby forming a sandwich structure, wherein the second ultra-thin nitride film is deposited using an atomic layer deposition (ALD) technique;
> completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure; and
> completing fabrication of the device. [Emphasis added.]
>
> 12. **(Amended)** A method of fabricating a semiconductor device, having a nitride/high-k material/nitride gate dielectric stack, comprising:
> initiating formation of the nitride/high-k material/nitride gate dielectric stack by:
> depositing **a first ultra-thin nitride film** on a semiconductor substrate,
> wherein the first ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique, and
> wherein the substrate comprises a silicon wafer or a silicon-on-insulator (SOI) wafer;
> depositing **a high-k material** on the first ultra-thin nitride film; and
> depositing **a second ultra-thin nitride film** on the high-k material, thereby forming a sandwich structure, wherein the second ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique;
> completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure; and
> completing fabrication of the device. [Emphasis added.]

Therefore, the Applicant respectfully requests that the Examiner's grounds for rejection on this basis be withdrawn.

II. Rejection of Claim 3, 7, 10, 13, and 15-19 under 35 U.S.C. §103(a).

The Examiner has rejected Claims 3, 7, 10, 13, and 15-19, under 35 U.S.C. §103(a), as being unpatentable over Gardner et al. (US 5,963,810), in view of Dautartas et al. (US 6,124,158), stating:

> Gardner discloses the claimed invention except: ... for where Dautartas discloses: ... wherein the nitride films are deposited by using an atomic layer deposition technique (col. 7, lns. 15-30). ... obvious ... to form the nitride layers using an ALD technique, because this deposition technique provides excellent uniformity and surface conformity of thin insulator films.

Notwithstanding Claims 1, 3, 7, 12, 13, and 15 being herein amended to better encompass the present invention, the Applicant respectfully traverses the Examiner's grounds for rejection on this basis. The Examiner concedes that "Gardner discloses the claimed invention except: ... for where Dautartas discloses: ... wherein the nitride films are deposited by using an atomic layer deposition technique." Gardner merely teaches depositing a silicon nitride (Si_3N_4) layer 303 and an optional silicon nitride capping layer by **sputtering** (col. 5, ll. 30-45; col. 6, ll. 40-42). In contrast, the Applicant teaches depositing silicon nitride layers 21 and 22 by an **atomic layer deposition (ALD)** technique (Spec., p. 3, l. 13, 20-21; herein amended Claims 1 and 12). As such, Gardner does not teach the presently claimed combination of method steps.

In addition, Gardner merely teaches a high dielectric constant material layer or high permittivity layer 305, comprising **barium strontium titanate ($Ba_{1-x}Sr_xO3$), tantalum oxide (Ta_xO_y), lead zinc niobate ($PbZn_xNb_{1-x}O_3$), and lead scandium tantalum oxide ($PbSc_xTa_{1-x}O_3$)**. In contrast, Claims 5, 6, and 14 collectively have the following limitation for forming the high dielectric constant material layer or thin metal film 30 which contains species not taught by Gardner: wherein the **thin metal film** comprises at least one metal selected from a group consisting essentially of **zirconium (Zr), hafnium (Hf), titanium (Ti), and tantalum (Ta)**, and wherein the **thin metal film** comprises **a metal oxide**. As such, the presently claimed thin metal film 30 contains a patentably distinct **group of species** *in combination with* **depositing silicon nitride layers** 21 and 22 by the patentably disctinct **atomic layer deposition (ALD)** technique.

Thus, Gardner does not teach, suggest, nor motivate the present combination of method steps in Claims 3, 7, 10, 13, and 15-19 which now subsume the limitations of the herein amended claims from which they depend (i.e., the limitations respectively recited in Claims 1 and 12, as discussed, supra). Therefore, the Applicant respectfully requests that the Examiner's grounds for rejection on this basis be withdrawn.

III. Rejection of Claim 3, 7, 10, 13, and 15-19 under 35 U.S.C. §103(a) is Improper under 35 U.S.C. §103(c).

Alternatively, the Applicant respectfully traverses the Examiner's grounds for rejection on the basis that the Gardner et al. (US 5,963,810) has been improperly combined, as a 35 U.S.C. §103(a) reference, with Dautartas under the provisions of 35 U.S.C.§103(c) which state:

> (c) Subject matter developed [1] by another person, [2] which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section [3] where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

With respect to the **first element of §103(c), MPEP 706.02(l), third paragraph,** states: "The term 'another' as used in 35 U.S.C. 103 means any entity other than the inventor and **would include the inventor and any other persons**." In Gardner et al. (US 5,963,810), the named inventors are Gardner, Gilmer, and Spikes, while in the present application (US 09/491,457), the named inventor is Yu. Therefore, the first element of §103(c) is satisfied.

With respect to the **second element of §103(c), MPEP 706.02(l), second paragraph,** states: "If the subject matter qualifies as prior art under any other subsection (e.g., ...102(a), 102(b), ..., it will not be disqualified as prior art under ... 103(c)." As discussed, supra, independent Claims 1 and 12 are herein amended to recite a claimed combination of method steps not taught by Gardner. Thus, Gardner is not a valid §102(b) reference. Therefore, the second element of §103(c) is satisfied.

With respect to the **third element of §103(c), MPEP §706.02(l)(2)** generally states the requirement that common ownership must be established at the time of the invention. **MPEP §706.02(l)(2)(II)**, in particular, states:

> The statement concerning common ownership should be **clear and conspicuous** (e.g., on a separate piece of paper **or in a *separately labeled section***) in order to ensure that the examiner quickly notices the statement. **Applicants *may, but are not required to,* submit further evidence, such as assignment records, affidavits or declarations by the common owner, or court decisions, in addition to the above-mentioned statement concerning common ownership.**

Here, the Applicants hereby reiterate that the common assignee, AMD, is readily apparent from the face of the Gardner patent. In addition, Gardner's recordation of assignment as well as that of the present invention to the common assignee, Advanced Micro Devices, Inc. are already of record in the USPTO. The Applicant hereby submits the explicit statement in the separately labeled section, for the record, in compliance with MPEP §706.02(l)(2)(II) as follows:

Common Ownership Statement

The subject matter of Gardner et al. (US 5,963,810), evident from the face of the patent, as well as that of the claimed invention (US 09/826,472) were *owned* by Advanced Micro Devices, Inc. (AMD) *and* were *subject to an obligation of assignment* to the same entity, AMD, *at the time the present invention was made.*

Thus, in light of common ownership evidence as well as the distinguishing evidence herein proffered, **the Applicants respectfully submit that Gardner,** upon which the Examiner relies to sustain the 35 U.S.C. §103(a) rejection, **does not qualify as a valid reference under 35 U.S.C. §102(b) nor under 35 U.S.C. §102(e); and the third element of §103(c) is satisfied. Therefore, the Applicants respectfully request that Gardner be disqualified as a 35 U.S.C. §103(a) cited reference, under 35 U.S.C. §103(c) and that the Examiner's ground for rejection on this basis be withdrawn.**

IV. Formal Drawing.

The Applicant respectfully requests that the Examiner kindly accept the herewith submitted formal Drawing.

CONCLUSION

Accordingly, the Title is herein amended, the Specification is herein amended, Claims 1, 3, 7, 12, 13, and 15 are herein amended, and Claim 20 is herein canceled, without prejudice, and the Abstract is herein amended to better encompass the full scope and breadth of the present invention, notwithstanding the Applicant's belief that the claims would have been allowable as originally filed. A marked-up version of the Specification, a marked-up version of the Claims, and a marked-up version of the Abstract are herewith submitted. Therefore, reconsideration of the present application in light of the foregoing amendment and these remarks is respectfully requested. ***The Examiner is further cordially invited to telephone the undersigned for any reason which would advance the pending claims to allowance.***

Respectfully submitted,

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MARKED-UP VERSION OF THE SPECIFICATION

In the Specification: Kindly amend the Specification as follows for style and clarity and for paragraph numbering. No new matter has been introduced.

PATENT
Docket No. P1296

TITLE OF THE INVENTION

METHOD OF FABRICATING A SEMICONDUCTOR DEVICE HAVING A NITRIDE/HIGH-K/NITRIDE GATE DIELECTRIC STACK BY ATOMIC LAYER DEPOSITION (ALD) [AND A DEVICE THEREBY FORMED]

CROSS-REFERENCE TO RELATED APPLICATION(S)

Not Applicable

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

Not Applicable

REFERENCE TO A MICROFICHE APPENDIX

Not Applicable

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to semiconductor devices and their methods of fabrication. More particularly, the present invention relates to the formation of gate stacks. Even more particularly, the present invention relates to forming a gate stack having superior thermal stability and reduced diffusion into silicon-bearing semiconductor structures.

2. Description of the Background Art

[0002] Currently, the semiconductor industry has an interest in reducing the critical dimensions of transistors. As such, the thickness of the gate oxide must also be reduced. In so doing, the

related art has faced problems associated with a significant increase in direct tunneling leakage current through a very thin gate oxide (i.e., < 25 Angstroms). In an effort to suppress the severe gate leakage current, a high dielectric constant (high-k) material may be used as a gate dielectric, replacing a conventional thermal oxide. Several high dielectric constant (high-k) materials (metal oxides) are good candidates for gate dielectric insulators: zirconia or zirconium dioxide (ZrO_2), hafnia or hafnium dioxide (HfO_2), titania or titanium dioxide (TiO_2), tantala or tantalum pentoxide (Ta_2O_5), and the like.

[0003] However, a high-k gate dielectric insulator, such as the foregoing metal oxides, must have a thickness which is much greater than that of a conventional thermal oxide to be similarly effective, because the direct current density is exponentially proportional to a dielectric layer's thickness. Thus, the direct tunneling current flow through a gate dielectric insulator may be significantly reduced, motivating its use in [for] very small transistors. Another major problem with using a high-k material is thermal instability. High-k materials tend to diffuse into the silicon (Si) substrate, a polysilicon (poly-Si) gate, or a polysilicon-germanium (poly-SiGe) gate during subsequent high temperature processing steps. Therefore, a need exists for a method of fabricating a semiconductor device having a high-k dielectric gate insulator with good thermal stability which does not diffuse into the Si substrate, the poly-Si gate, or the poly-SiGe gate when experiencing subsequent high temperature processes.

BRIEF SUMMARY OF THE INVENTION

[0004] Accordingly, the present invention provides a method of fabricating a semiconductor device comprising a high-k dielectric gate insulator having good thermal stability which does not diffuse into a Si substrate, a poly-Si gate, or a poly-SiGe gate when experiencing subsequent high temperature processes, and a device thereby formed. Generally, the present invention device has a high-k gate dielectric insulator (i.e., a nitride/high-k material/nitride gate dielectric stack) formed by atomic layer deposition (ALD). The present invention method for fabricating the present device, generally comprises: depositing a first ultra-thin nitride film; depositing a high-k material film; and depositing a second ultra-thin nitride film. The unique features of the present method basically involve a sandwich structure formed by depositing an ultra-thin nitride film, which may comprise silicon nitride (Si_3N_4), before and after depositing the high-k material film, which may comprise a thin metal film, whereby the first ultra-thin nitride film provides resistance

to metal diffusion into the Si substrate, the poly-Si gate electrode, or the poly-SiGe gate electrode. This present invention device, so formed, has the advantages of providing sufficient diffusion resistance as well as thermal stability in a thin (i.e., small) feature size.

[0005] By way of example, and not of limitation, a semiconductor device having a high-k dielectric gate insulator with good thermal stability which does not diffuse into a Si substrate, a poly-Si gate, or a poly-SiGe gate when experiencing subsequent high temperature processes, may be fabricated according to the present invention by: (a) providing a substrate, wherein the substrate may comprise a silicon wafer or a silicon-on-insulator (SOI) wafer; (b) initiating formation of a nitride/high-k material/nitride gate dielectric stack by depositing a first ultra-thin nitride film on the substrate, wherein the first ultra-thin nitride film may be deposited atomic layer deposition (ALD), and wherein the first ultra-thin nitride film may comprise 1 - 2 atomic layer(s) of silicon nitride (Si_3N_4); (c) depositing a high-k material, which may comprise a thin metal film, on the first ultra-thin nitride film, wherein the thin metal film may comprise at least one metal selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), titanium (Ti), and tantalum (Ta), wherein the thin metal film may also comprise a metal oxide; (d) depositing a second ultra-thin nitride film on the high-k material, thereby forming a sandwich structure, wherein the second ultra-thin nitride film may be deposited atomic layer deposition (ALD), and wherein the second ultra-thin nitride film may comprise 1 - 2 atomic layer(s) of silicon nitride (Si_3N_4); (e) completing formation of the nitride/high-k material/nitride gate dielectric stack, wherein the step (e) comprises (e)(1) depositing a thick gate material on the second ultra-thin nitride film, wherein the thick gate material may comprise a material selected from a group consisting essentially of polysilicon (poly-Si) and polysilicon-germanium (poly-SiGe); (e)(2) patterning the thick gate material, thereby forming a gate electrode; and (e)(3) etching portions of the sandwich structure uncovered by the gate electrode, thereby completing formation of the stack; and (f) completing fabrication of the semiconductor device, wherein step (f) may comprise the forming of a MOSFET structure comprising the stack, wherein the step (f) may further comprise (f)(1) forming a source/drain structure in the substrate and flanking the stack, (f)(2) forming at least one spacer on at least one sidewall of the stack, and (f)(3) silicidizing a shallow source/drain region of the substrate as well as the stack, thereby respectively forming a source/drain silicide in the shallow region and a gate silicide on the stack.

[0006] [An object] Advantages of the present invention [is to reduce] include the reduction of direct tunneling current flow through a gate dielectric insulator of a semiconductor device[.], [Another object of the present invention is to fabricate] and the fabrication of a semiconductor device comprising a high-k dielectric gate insulator having good thermal stability which does not diffuse into a Si substrate, a poly-Si gate, or a poly-SiGe gate when experiencing subsequent high temperature processes. Further [objects and] advantages of the invention will be [brought out] demonstrated in the following portions of the specification, wherein the detailed description is for the purpose of fully disclosing preferred embodiments of the invention without thereon placing limitations [thereon].

BRIEF DESCRIPTION OF THE DRAWING[(S)]

[0007] For a better understanding of the present invention, reference is made to the several figures of the below-referenced accompanying [drawing(s)] Drawing which is[/are for] illustrative in purpose[s] and where like reference numbers denote like elements.

[0008] FIG. 1 through FIG. 6, together, constitute a process flow diagram of the fabrication of a semiconductor device, in accordance with the present invention, wherein the semiconductor device is shown in cross-section at various stages of the process.

DETAILED DESCRIPTION OF THE INVENTION

[0009] Referring more specifically to the drawings for illustrative purposes, the present invention is embodied in the apparatus and method generally shown in FIG. 1 through FIG. 6. These figures depict an embodiment of a process for fabricating a semiconductor device comprising a high-k dielectric gate insulator having good thermal stability which does not diffuse into a Si substrate, a poly-Si gate, or a poly-SiGe gate when experiencing subsequent high temperature processes. Each figure illustrates a particular processing stage, and presents a side view in cross-section of the device at that stage of processing. However, that the apparatus may vary as to configuration and as to details of the parts, and that the method may vary as to the specific steps and sequence, without departing from the basic concepts as disclosed herein, will be appreciated.

[0010] Referring first to Figure 1, in the first stage of processing, a substrate 10 is provided, wherein the substrate 10 may comprise a silicon wafer or a silicon-on-insulator (SOI) wafer.

[0011] Next, as shown in Figure 2, a first ultra-thin nitride film 21 is deposited on the substrate 10, thereby initiating formation of a nitride/high-k material/nitride gate dielectric stack, wherein the first ultra-thin nitride film 21 may be deposited using an atomic layer deposition (ALD) technique, wherein the first ultra-thin nitride film 21 may comprise silicon nitride (Si_3N_4), and wherein the first ultra-thin nitride film 21 may a thickness in a range of 1 - 2 atomic layer(s).

[0012] Next, as shown in Figure 3, a high-k material, such as a thin metal film 30, is deposited on the first ultra-thin nitride film 21, wherein the thin metal film 30 may comprise at least one metal selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), titanium (Ti), and tantalum (Ta), wherein the thin metal film 30 also comprises a metal oxide.

[0013] Next, as shown in Figure 4, a second ultra-thin nitride film 22 is deposited on the high-k material (e.g., the thin metal film 30), thereby forming a sandwich structure 35, wherein the second ultra-thin nitride film 22 may be deposited using am atomic layer deposition (ALD) technique, and wherein the second ultra-thin nitride film 22 may comprise silicon nitride (Si_3N_4), and wherein the second ultra-thin nitride film 22 may have a thickness in a range of 1 - 2 atomic layer(s).

[0014] Next, as shown in Figure 5, a completed nitride/high-k material/nitride gate dielectric stack 40 is formed on the substrate 10, wherein the stack 40 is completed by depositing a thick gate material 31 on the second ultra-thin nitride film 22, wherein the thick gate material 31 may comprise a material selected from a group consisting essentially of polysilicon (poly-Si) and polysilicon-germanium (poly-SiGe); patterning the thick gate material 31 with a material such as a photoresist (not shown), thereby forming a gate electrode 32; and etching portions of the sandwich structure 35 uncovered by the gate electrode 32, thereby forming the nitride/high-k material/nitride gate dielectric stack 40.

[0015] As depicted in Figure 6, a MOSFET structure 50 comprises the stack 40, wherein the MOSFET structure 50 further comprises a source/drain structure 51 formed in the substrate 10 and flanking the stack 40, at least one spacer 52 formed on at least one sidewall of the stack 40, and a shallow source/drain region 15 as well as the nitride/high-k/nitride gate dielectric stack 40 being silicidized to respectively form a source/drain silicide 16 in the shallow region 15 of the substrate 10 and a gate silicide 41 on the stack 40.

[0016] Information as herein shown and described in detail is fully capable of attaining the above-described object of the invention, the presently preferred embodiment of the invention, and is, thus, representative of the subject matter which is broadly contemplated by the present invention. The scope of the present invention fully encompasses other embodiments which may become obvious to those skilled in the art, and is to be limited, accordingly, by nothing other than the appended claims, wherein reference to an element in the singular is not intended to mean "one and only one" unless explicitly so stated, but rather "one or more." All structural and functional equivalents to the elements of the above-described preferred embodiment and additional embodiments that are known to those of ordinary skill in the art are hereby expressly incorporated by reference and are intended to be encompassed by the present claims.

[0017] Moreover, no requirement exists for a device or method to address each and every problem sought to be resolved by the present invention, for such to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims. However, it should be readily apparent to those of ordinary skill in the art that various changes and modifications in form, semiconductor material, and fabrication material detail may be made without departing from the spirit and scope of the inventions as set forth in the appended claims. No claim herein is to be construed under the provisions of 35 U.S.C. §112, sixth paragraph, unless the element is expressly recited using the phrase "means for."

MARKED-UP VERSION OF THE CLAIMS

In the Claims:

A. Kindly cancel non-elected Claim 20, without prejudice.

B. Kindly amend Claims 1, 3, 7, 12, 13, and 15, as follows. No new matter has been introduced.

1. **(Amended)** A method of fabricating a semiconductor device, having a nitride/high-k material/nitride gate dielectric stack, comprising:

initiating formation of the nitride/high-k material/nitride gate dielectric stack by:

depositing a first ultra-thin nitride film on a semiconductor substrate, wherein the first ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique;

depositing a high-k material on the first ultra-thin nitride film; and

depositing a second ultra-thin nitride film on the high-k material, thereby forming a sandwich structure, wherein the second ultra-thin nitride film is deposited using an atomic layer deposition (ALD) technique;

completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure; and

completing fabrication of the device.

2. A method as recited in claim 1, wherein the substrate comprises a silicon wafer or a silicon-on-insulator (SOI) wafer.

3. **(Amended)** A method as recited in claim 1,

[wherein the first ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique, and]

wherein the first ultra-thin nitride film comprises silicon nitride (Si_3N_4), and

wherein the first ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s).

4. A method as recited in claim 1, wherein the high-k material comprises a thin metal film.

5. A method as recited in claim 1, wherein the thin metal film comprises at least one metal selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), titanium (Ti), and tantalum (Ta).

6. A method as recited in claim 1, wherein the thin metal film comprises a metal oxide.

7. **(Amended)** A method as recited in claim 1,
[wherein the second ultra-thin nitride film is deposited using an atomic layer deposition (ALD) technique, and]
wherein the second ultra-thin nitride film comprises siliçon nitride (Si_3N_4), and
wherein the second ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s).

8. A method as recited in claim 1, wherein completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure comprises:
depositing a thick gate material on the second ultra-thin nitride film;
patterning the thick gate material, thereby forming a gate electrode; and
etching portions of the sandwich structure uncovered by the gate electrode, thereby completing formation of the nitride/high-k material/nitride gate dielectric stack

9. A method as recited in claim 1, wherein completing fabrication of the device comprises forming of a MOSFET structure comprising the gate dielectric stack.

10. A method as recited in claim 8,
wherein the thick gate material comprises a material selected from a group consisting essentially of polysilicon (poly-Si) and polysilicon-germanium (poly-SiGe), and
wherein the thick gate material is patterned using a material such as photoresist.

11. A method as recited in claim 1, wherein completing fabrication of the device comprises:
forming a source/drain structure in the substrate and flanking the gate dielectric stack;
forming at least one spacer on at least one sidewall of the gate dielectric stack; and
silicidizing a shallow source/drain region as well as the high-k gate stack, thereby forming a source/drain silicide in a shallow source/drain region of the substrate and a gate silicide on the gate dielectric stack.

12. **(Amended)** A method of fabricating a semiconductor device, having a nitride/high-k material/nitride gate dielectric stack, comprising:
initiating formation of the nitride/high-k material/nitride gate dielectric stack by:
depositing a first ultra-thin nitride film on a semiconductor substrate,
wherein the first ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique, and
wherein the substrate comprises a silicon wafer or a silicon-on-insulator (SOI) wafer;
depositing a high-k material on the first ultra-thin nitride film; and
depositing a second ultra-thin nitride film on the high-k material, thereby forming a sandwich structure, wherein the second ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique;
completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure; and
completing fabrication of the device.

13. **(Amended)** A method as recited in claim 12,
[wherein the first ultra-thin nitride film is deposited by using an atomic layer deposition (ALD) technique, and]
wherein the first ultra-thin nitride film comprises silicon nitride (Si_3N_4), and
wherein the first ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s).

14. A method as recited in claim 13,
wherein the high-k material comprises a thin metal film,
wherein the thin metal film comprises at least one metal selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), titanium (Ti), and tantalum (Ta), and
wherein the thin metal film comprises a metal oxide.

15. **(Amended)** A method as recited in claim 14,
[wherein the second ultra-thin nitride film is deposited using an atomic layer deposition (ALD) technique, and]
wherein the second ultra-thin nitride film comprises silicon nitride (Si_3N_4), and
wherein the second ultra-thin nitride film has a thickness in a range of 1 to 2 atomic layer(s).

16. A method as recited in claim 15, wherein completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure comprises:
depositing a thick gate material on the second ultra-thin nitride film;
patterning the thick gate material, thereby forming a gate electrode; and
etching portions of the sandwich structure uncovered by the gate electrode, thereby completing formation of the nitride/high-k material/nitride gate dielectric stack

17. A method as recited in claim 16, wherein completing fabrication of the device comprises forming of a MOSFET structure comprising the gate dielectric stack.

18. A method as recited in claim 17,
wherein the thick gate material comprises a material selected from a group consisting essentially of polysilicon (poly-Si) and polysilicon-germanium (poly-SiGe), and
wherein the thick gate material is patterned using a material such as photoresist.

19. A method as recited in claim 18, wherein completing fabrication of the device comprises:

forming a source/drain structure in the substrate and flanking the gate dielectric stack;

forming at least one spacer on at least one sidewall of the gate dielectric stack; and

silicidizing a shallow source/drain region as well as the high-k gate stack, thereby forming a source/drain silicide in a shallow source/drain region of the substrate and a gate silicide on the gate dielectric stack.

MARKED-UP VERSION OF THE ABSTRACT

In the Abstract: **Kindly amend the Abstract as follows. No new matter has been introduced.**

ABSTRACT

A method of fabricating a semiconductor device, having a nitride/high-k material/nitride gate dielectric stack with good thermal stability which does not diffuse into a silicon substrate, a polysilicon gate, or a polysilicon-germanium gate when experiencing subsequent high temperature processes, involving: (a) providing a substrate; (b) initiating formation of the nitride/high-k material/nitride gate dielectric stack by depositing a first ultra-thin nitride film on the substrate; (c) depositing a high-k material, such as a thin metal film, on the first ultra-thin nitride film; (d) depositing a second ultra-thin nitride film on the high-k material, thereby forming a sandwich structure; (e) completing formation of the nitride/high-k material/nitride gate dielectric stack from the sandwich structure; and (f) completing fabrication of the semiconductor device[, and a device thereby formed].